REMARKS

I. Introduction

A three-month extension of time to respond to the March 17, 2003 Office Action is hereby respectfully requested. A check in the amount of $930.00 is enclosed in payment of the three-month extension-of-time fee.

The specification has been amended to correct minor and obvious typographical errors.

Claims 2 and 13 have been cancelled without prejudice.

Claims 1, 6, 9, 11, and 14 have been amended to more particularly define the claimed invention and to update resulting claim dependancies.

No new matter has been added by the amendments to the specification and claims.

Claims 3-5, 7, 8, 10, 12, and 15-26 are also pending in the case.

Reconsideration of this application in light of the following Remarks is hereby respectfully requested.

II. The Objections to the Claims

The Examiner objected to claims 19, 20, 23, and 24 under 37 C.F.R. § 1.75(c) "as being of improper dependent form for failing to further limit the subject matter of a previous claim" (Office Action, page 2, lines 3 and 4). However, § 2173.05(f) of the Manual of Patent Examining Procedure (M.P.E.P.) states that "[a] claim which makes reference to a preceding claim to define a limitation is an acceptable claim construction which should not necessarily be rejected as improper." Claim 19 defines voltage controlled oscillator circuitry in which a

plurality of the delay cells of claim 18 are connected in a closed loop series, and is therefore not improper under 37 C.F.R. § 1.75(c) for simply referring back to claim 18. Accordingly, withdrawal of the 37 C.F.R. § 1.75(c) objection with respect to claim 19 is respectfully requested. Furthermore, withdrawal of the 37 C.F.R. § 1.75(c) objection with respect to claims 20, 23, and 24 is respectfully requested for the same reasons as those above with respect to claim 19.

III. The Rejections Based on 35 U.S.C. § 102

Claims 1, 3-5, 7-12, and 15-19 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Huizer, U.S. Patent 5,477,182 (hereinafter "Huizer"). Claims 1, 3-12, 14-22, and 24 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshihiro et al., European Patent EP 0 987 822 A2 (hereinafter "Yoshihiro"). The Examiner's rejections are respectfully traversed.

Applicants' claimed invention of independent claim 1, as amended, defines a delay cell that includes a switching transistor (e.g., transistor SW1 of FIG. 4) connected in series between a plurality of load resistance transistors (e.g., transistors RL1a, RL1b, ..., RL1n of FIG. 4) and a plurality of bias current transistors (e.g., transistors ICONTa, ICONTb, ..., ICONTn of FIG. 4), switching circuitry (e.g., multiplexer 110b of FIG. 4) "configured to selectively operatively connect at least one of the load resistance transistors in parallel with at least one other of the load resistance transistors," and further switching circuitry (e.g., multiplexer 120b of FIG. 4) "configured to selectively operatively connect at least one of the bias current transistors in parallel with

at least one other of the bias current transistors." These two switching circuitries of the present invention allow "the number of the load resistance transistors that are actually operating in parallel to be selected" and allow "the number of bias current transistors that are actually operating in parallel to be similarly selected," respectively, which "allows the operating range (i.e., the time delay characteristic) of the delay cell to be greatly extended" (applicants' specification, page 2, lines 12-20). Also see applicant's specification, page 9, lines 30-33, for example.

The Yoshihiro Rejection

Yoshihiro, on the other hand, relates to a "PLL circuit [that] detects [an] oscillation halt of a voltage control oscillator" that is structured by "a ring oscillator in which a plurality of differential amplifiers are connected in a ring form. A plurality of oscillation control means are arranged for the respective inputs of the differential amplifiers so as to set the ring oscillator into an oscillationable state when the voltage control oscillator halts" (Yoshihiro, Abstract). Yet, the Examiner alleges that

> FIG. 7 of Yoshihiro shows a differential delay cell comprising a plurality of load transistors (750, 755) connectable in parallel with one another, a plurality of bias current transistors (754, 757) connectable in parallel with one another, [and] switching circuitry (not shown) producing control voltage (707) to selectively operatively connect at least one of the load transistors [750, 755] in parallel with at least one other of the load transistors as called for in [applicants'] claims 1, 7-12, 17-22 and 24 (Office Action, page 3, lines 13-17).

Applicants respectfully disagree.

Nowhere does Yoshihiro show or suggest "switching circuitry configured to selectively operatively connect" at least one load resistance transistor in parallel with one other load resistance transistor. Specifically, Yoshihiro's terminal 707 does not selectively connect transistor 755 in parallel with transistor 750 when desired, but instead always keeps transistor 755 in the ON state, even when transistor 750 is put in the OFF state when an oscillation halts.

> [V]oltage is always applied to the control input terminals 707, 708 of the transistors 755-757 which are connected to these transistors [750, 751, 754] in parallel so that the current always flows.
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> . . .
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> . . . When the control input terminals 701,704 [voltage 103] approaches the power supply line VDD or the ground line GND in the transistors 750, 751, 754, the transistors 750, 751, 754 become the OFF state and no current flows. However, the current always flows along the transistors 755-757. Consequently, the circuit can operate as the differential amplifier.
> (Yoshihiro, column 16, lines 44-54).

Therefore, because Yoshihiro's transistor 755 is always in the ON state because voltage is always applied to terminal 707, transistor 750 is put into the OFF state when voltage 103 (i.e., converted voltage of phase difference signal 102) approaches VDD or GND. Nothing like the "switching circuitry configured to selectively operatively connect" at least one of the load resistance transistors in parallel with at least one other of the load resistance transistors, thus defined by applicants' claim 1, is shown or suggested in Yoshihiro.

Applicants' independent claim 11 is patentable over Yoshihiro for at least the same reasons claim 1 is patentable over Yoshihiro. Specifically, the delay cell of claim 11 defines a plurality of load resistance transistors connected in parallel with one another, and switching circuitry configured to "selectively apply" either a substantially fixed deactivating control signal or a variable activating control signal to at least one of the load resistance transistors.

Furthermore, applicants' independent claim 17 is patentable over Yoshihiro for at least the same reasons claim 1 is patentable over Yoshihiro. Specifically, the delay cell of claim 17 defines a plurality of first load resistance transistors connected in parallel with one another, and first switching circuitry configured to "selectively activate" at least one of the first load resistance transistors for operation in parallel with at least one other of the first load resistance transistors.

Claims 1, 11, and 17 are therefore not anticipated by Yoshihiro. Applicants respectfully submit that independent claims 1, 11, and 17, and any claims dependent therefrom, are allowable over Yoshihiro.

The Huizer Rejection

The Examiner alleges that

> FIG. 3 of Huizer shows a differential delay cell comprising a plurality of load transistors (CL1, L1) connectable in parallel with one another, a plurality of bias current transistors (S) connectable in parallel with one another, . . . [and] switching circuitry (not shown) producing control voltage (c1, c2, c1/, c2/) to selectively operatively connect at least one of the load transistors [CL1, L1] in parallel with at least

> one other of the load transistors as called for in [applicants'] claims 1, 7-12, and 17-19 (Office Action, page 3, lines 13-17).

Applicants' independent claim 1 has been amended to define "further switching circuitry configured to selectively operatively connect at least one of the bias current transistors in parallel with at least one other of the load resistance transistors," (e.g., multiplexer 120b of FIG. 4) in addition to the "switching circuitry configured to selectively operatively connect at least one of the load resistance transistors in parallel with at least one other of the load resistance transistors." Therefore, claim 1 provides for separate switching circuitries for selectively operatively connecting load resistance transistors and bias current transistors, respectively.

Nowhere does Huizer show or suggest "switching circuitry configured to selectively operatively connect" load resistance transistors in parallel and "further switching circuitry configured to selectively operatively connect" bias current transistors in parallel, as required by applicants' amended claim 1. Instead, Huizer shows switching voltages C1 and C2 are applied not only to load circuits L1 and L2, but also to tail current circuit S. Therefore, Huizer's load circuit L1 and tail current circuit S do not each have their own switching circuitry configured to selectively operatively connect at least one of its transistors in parallel with at least one other of its transistors, but instead share the same switching voltages C1 and C2. Nothing like the "switching circuitry"

and the "further switching circuitry," thus defined by applicants' claim 1, is shown or suggested in Huizer.

Applicants' independent claim 11 is patentable over Huizer for at least the same reasons claim 1 is patentable over Huizer. Specifically, the delay cell of claim 11 has been amended to define a plurality of load resistance transistors connected in parallel with one another, a plurality of bias current transistors connected in parallel with one another, switching circuitry configured to "selectively apply" either a substantially fixed deactivating control signal or a variable activating control signal to at least one of the load resistance transistors, and "further switching circuitry configured to selectively apply either a substantially fixed disabling control signal or a variable enabling control signal to at least one of the bias current transistors."

Furthermore, applicants' independent claim 17 is patentable over Huizer for at least the same reasons claim 1 is patentable over Huizer. Specifically, the delay cell of claim 17 defines a plurality of first load resistance transistors connected in parallel with one another, a plurality of bias current transistors connected in parallel with one another, "first switching circuitry configured to selectively activate" at least one of the first load resistance transistors for operation in parallel with at least one other of the first load resistance transistors, and "second switching circuitry configured to selectively activate at least one of the bias current transistors for operation in parallel with at least one other of the bias current transistors."

Claims 1, 11, and 17 are therefore not anticipated by Huizer. Applicants respectfully submit that

independent claims 1, 11, and 17, and any claims dependent therefrom, are allowable over Huizer.

IV. The Rejection Based on 35 U.S.C. § 103

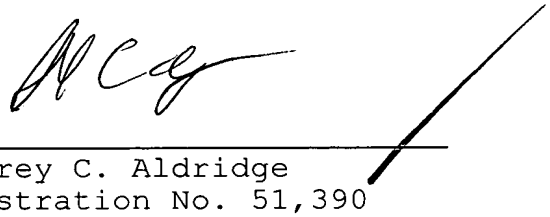
Claims 23-26 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshihiro. The Examiner's rejection is respectfully traversed.

As applicants have pointed out above, independent claim 17 is allowable over Yoshihiro. Thus, for at least the foregoing reasons, claims 23-26, which depend from claim 17, are therefore also allowable over Yoshihiro. Accordingly, applicants respectfully request that the rejection of claims 23-26 also be withdrawn.

V. Conclusion

The foregoing demonstrates that claims 1, 3-12, and 14-26 are allowable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,



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